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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,426	10/20/2003	Jae-Hyun Park	5649-1163	2795

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,426	PARK, JAE-HYUN	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *16-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-15,22-24,26,28 and 29* is/are rejected.

7)☒ Claim(s) *5,25 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

In the Response to Restriction/Election Requirement dated June 9, 2005, Applicant has elected Species **I**, corresponding to Claims **1-15 and 22-29**. This election is made with traverse, because Applicant submits that Claims **22-29** are generic to both Species **I** and Species **II** (Claims **16-21**) is acknowledged. Accordingly, Claims **16-21** are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected Claims **16-21**.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) based on an application filed in REPUBLIC OF KOREA, 2003-0030353 on 05/13/2003.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 10/20/2003. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims **1-4, 6-12, 14, 15, 22, 23, 26, 28 and 29** are rejected under 35 U.S.C. 102(b) as being anticipated by Nishimura et al. (US Pub. 2002/0036917 hereinafter referred to as "Nishimura"), Applicant's submitted prior art (ASPA).

Regarding Claim **1**, Nishimura discloses in Figs. 1-2 and 39, and the corresponding texts as set forth in paragraphs [0006], [0007] and [0076]-[0115], a magnetic random access memory cell, comprises:

first and second sub-digit lines/write lines 10 disposed over a semiconductor substrate 1, the first and second sub-digit lines/write lines being spaced apart from each other when viewed from a top plan view (Fig. 2); and

a magnetic resistor 9 disposed over the first and second sub-digit lines/write lines and overlapping with the first and second sub-digit lines/write lines (Fig. 1), wherein the magnetic resistor is electrically connected to a predetermined region 3 of the semiconductor substrate through a magnetic resistor contact hole 5 that penetrates a gap region between the first and second sub-digit lines/write lines (Fig. 39).

Regarding Claims **2, 14 and 26**, Nishimura discloses in Fig. 2 the magnetic resistor has a length and a width smaller than the length when viewed from a top plan view, and the magnetic

resistor is disposed to cross over the first and second sub-digit lines/write lines along the length thereof.

Regarding Claims **3-4 and 12**, Nishimura discloses in Figs. 1-2 and 39 the first and second sub-digit lines/write lines extend parallel to each other (Fig. 2) wherein a direction of a current flowing in the first sub-digit line/write line is identical to a direction of a current flowing in the second sub-digit line/write line.

Regarding Claim **8**, Nishimura discloses in Figs. 1-2 and 39 a magnetic random access memory cell further comprises a bit line 6 which is disposed over the magnetic resistor and is electrically connected to the magnetic resistor, wherein the bit line is disposed to cross over the sub-digit lines/write lines.

Regarding Claims **9 and 15**, Nishimura discloses in Fig. 39 the magnetic resistor comprises a magnetic tunnel junction including a pinning layer, a pinned layer, a tunneling layer and a free layer which are sequentially stacked, and the pinned layer and the free layer comprise ferromagnetic layers having magnetic spins arrayed in a horizontal direction.

Regarding Claim **10**, Nishimura discloses in Figs. 1-2 and 39, and the corresponding texts as set forth in paragraphs [0006], [0007] and [0076]-[0115], a magnetic random access memory cell, comprises:

an access MOS transistor 4 at a predetermined region of a semiconductor substrate 1;

first and second parallel sub-digit lines/write lines 10 disposed over the access MOS transistor;

a magnetic resistor 9 disposed over the first and second sub-digit lines/write lines to overlap with the first and second sub-digit lines/write lines (Fig. 1), the magnetic resistor being

electrically connected to a drain region 3 of the access MOS transistor through a magnetic resistor contact hole 5 that penetrates a gap region between the first and second sub-digit lines/write lines (Fig. 39); and

a bit line 6 disposed over the magnetic resistor and electrically connected to the magnetic resistor, wherein the bit line crosses over the first and second sub-digit lines/write lines.

Regarding Claim **11**, Nishimura discloses in Figs. 1-2 and 39 a magnetic random access memory cell further comprising a common source line 12 electrically connected to a source region 2 of the access MOS transistor, wherein the common source line extends parallel to the sub-digit lines/write lines.

Regarding Claim **22**, Nishimura discloses in Figs. 1-2 and 39, and the corresponding texts as set forth in paragraphs [0006], [0007] and [0076]-[0115], a magnetic random access memory cell, comprises:

an MRAM substrate 1;

a magnetic resistor 9 on the MRAM substrate; and

first and second digit lines/write lines 10 between the magnetic resistor and the MRAM substrate and extending beneath the magnetic resistor (Fig. 39).

Regarding Claim **23**, Nishimura discloses in Figs. 1-2 and 39 an MRAM cell further comprises a magnetic resistor contact plug 5 that electrically contacts the magnetic resistor and extends from the magnetic resistor towards the MRAM substrate, between the first and second digit lines/write lines (Fig. 39).

Regarding Claim **28**, Nishimura discloses in Figs. 1-2 and 39 an MRAM cell further comprises a transistor 4 in the MRAM substrate and electrically connected to the magnetic resistor contact plug 5.

Regarding Claim **29**, Nishimura discloses in Figs. 1-2 and 39 the first and second digit lines/write lines are electrically connected in parallel.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **13 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (US Pub. 2002/0036917 hereinafter referred to as "Nishimura"), Applicant's submitted prior art (ASPA) in view of Matsuoka et al. (USP 6,560,135 hereinafter referred to as "Matsuoka").

Regarding Claim **13**, Nishimura discloses all the claimed limitations except for a magnetic random access memory cell further comprises spacers and capping layers covering the sidewalls and top surfaces of the sub-digit lines respectively, wherein the magnetic resistor contact hole extends between adjacent spacers and between the capping layers. Matsuoka discloses in Fig. 8 that an MRAM comprises spacers 1401 and capping layers 1402 covering the sidewalls and top surfaces of the sub-digit lines/writing word lines 702 respectively, wherein the

magnetic resistor contact hole 1105 extends between adjacent spacers and between the capping layers (col. 2, lines 35-56, col. 5, line 50-col. 7, line 13. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form an MRAM comprises spacers and capping layers covering the sidewalls and top surfaces of the sub-digit lines respectively, wherein the magnetic resistor contact hole extends between adjacent spacers and between the capping layers, as taught by Matsuoka in order for obtaining a self-aligned process.

Regarding Claim **24**, Nishimura discloses all the claimed limitations except for an MRAM cell further comprises first and second sidewall spacers, a respective one of which is on a sidewall of the respective first and second digit lines and face one another, and wherein the magnetic resistor contact plug extends between the first and second sidewall spacers. Matsuoka discloses in Fig. 8 that an MRAM comprises first and second sidewall spacers 1401, a respective one of which is on a sidewall of the respective first and second digit lines/writing word lines 702 and face one another, and wherein the magnetic resistor contact plug 1105 extends between the first and second sidewall spacers. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form an MRAM cell further comprises first and second sidewall spacers, a respective one of which is on a sidewall of the respective first and second digit lines and face one another, and wherein the magnetic resistor contact plug extends between the first and second sidewall spacers, as taught by Matsuoka in order for obtaining a self-aligned process.

Allowable Subject Matter

Claims **5, 25 and 27** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. The prior art of record, taken alone or in combination, fails to teach or suggest a magnetic random access memory cell wherein the first and second sub-digit lines extend parallel to each other and contact each other beyond the magnetic resistor, to form a single merged digit line having an opening beneath the magnetic resistor, and wherein the magnetic resistor contact hole penetrates the opening as recited in claim **5**; an MRAM cell wherein the first and second digit lines merge into a single digit line beyond the magnetic resistor as recited in claim **25**; and an MRAM cell further comprises a merged digit line between the magnetic resistor and the MRAM substrate, extending beneath the magnetic resistor and including therein a hole beneath the magnetic resistor that defines the first and second digit lines beneath the magnetic resistor as recited in claim **27**.

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ah

06/15/05

Andy Huynh

Patent Examiner